

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

### **REMARKS**

Claims 1-10 are pending in the application.

Claims 1 and 9 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated February 28, 2003.

### **Claim Objections**

Claims 1-20 are objected to because of minor informalities.

Independent claims 1 and 9 are amended, as needed, to overcome this objection. Reconsideration and withdrawal of this objection are respectfully requested.

### **Claim Rejections under 35 USC §103**

Claims 1-10 are rejected under 35 USC §103(a) as being unpatentable over Kitamura.

One of the objectives of the present invention is to prevent waste of raw materials. This objective can be achieved by fully utilizing leftover raw materials. Figures 4 and 7 provide a concrete example of how leftover raw materials for a particular shape can be preserved to be utilized for other shapes in the future. As shown in Figure 4, there is a total quantity of ten pieces needed for drawing number E320-1234-T567/01 design, one piece for order number 1 and nine pieces for order number 2.

However, your understanding of Fig 7 shows the layout in the predetermined manufacturing blocks (namely, raw material), in the case of producing a total of ten pieces of printed wiring boards

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

for drawing number E320-1234-T567 design (hereinafter referred to as "printed wiring boards for design 1"). In this case, four pieces of printed wiring boards for design 1 can be laid out in each block. Thus, in order to produce ten pieces of printed wiring boards for design 1, three pieces of predetermined manufacturing blocks are needed. In such case, the third block has a leftover portion, in which two more pieces of printed wiring boards for design 1 (illustrated with question marks) can be laid out. Two pieces of printed wiring boards for design 1 (illustrated with hatching), which are laid out on the third block, are called "fractional printed wiring boards". Therefore, each term of "the fraction" and "the fractional printed wiring board" does not mean the leftover raw material. The two pieces of printed wiring boards, which are laid out in the third block as shown in Fig. 7, will be re-laid out in the predetermined manufacturing block, together with other printed wiring boards, which are in the same manufacturing condition.

The present invention focuses on problem that when producing a predetermined number of printed wiring boards of multiple types according to an order, and laying out the printed wiring boards in the blocks (raw materials) per type, there arises waste of materials. That is, if it is required to produce only one piece of printed wiring board of a certain type, while four pieces of the printed wiring boards of the same type can be laid out in one block (raw material), which is used for producing the printed wiring boards at a maximum, the leftover portion (in which three more pieces of printed wiring boards of the same type can be laid out) will be wasted.

Further, as shown in Fig. 7, in the case where a predetermined number of the printed wiring boards of a certain type to be produced are laid out in one or more blocks (materials), and any of the blocks has a leftover portion(s), in which the printed wiring board(s) of the same type or different

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

types can be laid out, the left over portion(s) will be wasted.

In the present invention, the printed wiring board, which is laid out in the block having a leftover portion, is defined as "the fractional printed wiring board". A plurality of fractional printed wiring boards are collected and divided into multiple groups according to the respective manufacturing conditions, and layout in the blocks is performed respectively for each group. Thereby, the printed wiring boards of the different types in the same manufacturing condition are laid out in one block, so that waste of materials can be reduced.

"A fractional print wiring board" is defined in claim 2. Specifically, in the case where a manufacturing quantity of the printed wiring boards of a certain type cannot be divided completely by a maximum number of the printed wiring boards which can be laid out in a single predetermined manufacturing block, the term "the fractional print wiring board" means the printed wiring boards corresponding to a number smaller than the above maximum number or the remainder(s) of the division.

In the Office Action, Item 3-2, the Examiner asserted that "a predetermined manufacturing block" of the present invention corresponds to "a certain processing equipment" of Kitamura. However, "a predetermined manufacturing block" of the present invention is a raw material to be used for producing the printed wiring board.

In items 3-4 and 3-5, the Examiner is of the opinion that a grouping unit and a determining unit are obvious from the central processor (1101), which necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and the process information. However, dividing the

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

quantities of product into efficient lot sizes is a completely different process from dividing the fractional printed wiring boards into multiple groups according to the manufacturing conditions and laying out the fractional printed wiring boards in the predetermined manufacturing blocks (raw material) for each group. The central processor (1101) of Kitamura divides the quantities of product into efficient lot sizes, in order to prevent a load from concentrating on certain equipment. In the present invention, the detecting unit, the grouping unit and the determining unit perform the claimed processes for the fractional printed wiring board, in order to eliminate waste of raw materials. Thus, the present invention is completely different from Kitamura in respect to its objective and concrete constitution. Further, Kitamura does not at all show any teaching nor suggestion relating to the fractional printed wiring board.

In rejecting the claimed invention, the outstanding Office Action has substantially copied the claim language of the present invention and selectively provided insertions alleging where the same claimed element or claimed step is taught or suggested in the asserted prior art. However, the outstanding Office Action has consistently failed to assert any evidence where in the asserted prior art is there any teaching or suggestion of that the alleged system or method is concerned with any fractional printed wiring board.

More specifically, the claim language has correspondingly in independent claims 1 and 9 stated in relevant part that:

“a detecting unit detecting a fractional printed wiring board which should be laid out to a single predetermined manufacturing block together with a printed wiring board having a different type within the printed wiring boards scheduled to be manufactured on the basis of the manufacturing schedule data stored in said schedule data storage unit;” and

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

"detecting a fractional printed wiring board which should be laid out to a single predetermined manufacturing block together with a printed wiring board having a different type within the printed wiring boards scheduled to be manufactured on the basis of the manufacturing schedule data".

These aspects of the claimed invention is fully supported by way of examples in Figures 3 and 5, reference numeral 31, Figures 6-7, step S103, and associated written specification.

In rejecting these aspects of the claimed invention, the outstanding Office Action has stated in relevant part that:

"a detecting unit (205) detecting a quantity of printed wiring boards which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing schedule data; (Note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment). Note also figure 11, in which product information (1103), equipment information (1104) and a manufacturing situation (1105) are stored in memory and that network (1108) is connected to processing equipment (1110). See col. 8, lines 36-67".

In attempting to substantiate the Office position, the Office has specifically cited column 8, lines 36-67 of Kitamura, which portion has specifically stated in its entirety that:

"The central processing system 1101 is connected through a network 1108 to a semiconductor device manufacturing equipment 1110 provided in a production line 1109, and sequentially transmits product processing information through the network 1108.

FIG. 12 illustrates one example of the structure of information stored in the manufacturing situation memory 1105.

In the manufacturing situation memory 1105, the product data base 1201 storing the product name of the product being manufactured in the manufacturing line 1109 is linked with a lot number data base 1202, 1202A storing the lot number in a work-in-progress condition of each product which has already started to be manufactured. The lot number data base 1202 is linked to a working situation data base 1203, 1203A

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

storing the working situation of each lot.

Now, an operation of the second embodiment of the present invention will be described with reference to a flow chart of FIG. 13.

A signal indicating that for example a contamination trouble has occurred in the production line 1109, is transmitted to the central processing system 1101 through the network 1108 (step 1301).

Then, the process procedure of the product in which contamination trouble has occurred, is moved from the product information memory 1103 to the temporary memory 1106 (step 1302).

Thereafter, a flag is stood in the lot number data base 1202 of the problematic product. If the flag is stood, even if it is requested to perform the working in the equipment 1110, the equipment does not acknowledge the request, and therefore, the working can no longer advance (step 1303)."

In neither the stated Office position nor the Office asserted portion of Kitamura is there any teaching or suggestion of fractional material being utilized in this part of the manufacturing system or process.

The claim language has correspondingly in independent claims 1 and 9 stated in relevant part that:

"a grouping unit grouping each fractional printed wiring board detected by said detecting unit into any of groups according to the manufacturing condition data stored in said condition data storage unit;" and

"grouping each detected fractional printed wiring board into any of groups according to the manufacturing condition data".

These aspects of the claimed invention are fully supported by way of an example in Fig. 3 reference numeral 31, Figs. 6 and 8, step S104.

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

In rejecting these aspects of claims 1 and 9, the outstanding Office Action further asserted that:

"a dividing unit dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data; (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that such a system as described by Kitamura would necessarily be expected to group particular product based on a wide variety of criteria, including the particular process required, the particular model of board, as well as the manufacturing load on a particular piece of equipment See col. 9, lines 22-27, for example.)"

The outstanding Office Action substantiates its position by citing column 9, lines 22-27 of Kitamura, which portion has specifically stated in its entirety that:

"In another advantage of the present invention, since the equipment load is calculated on the basis of the actual working history and the work is distributed over the working equipment on the basis of the result of calculation, a load is never concentrated onto a limited equipment, and therefore, the production can be performed efficiently."

Again, in neither the stated Office position nor the Office asserted portion of Kitamura is there any teaching or suggestion of fractional material being utilized in this part of the manufacturing system or process.

The claim language has correspondingly in independent claims 1 and 9 stated in relevant part that:

"a determining unit determining, per group, layout to at least one predetermined manufacturing block of the fractional printed wiring board"; and

"determining, per group, layout to at least one predetermined manufacturing block of the fractional printed wiring board."

In rejecting these aspects of claims 1 and 9, the outstanding Office Action further stated in

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

relevant part that:

"a determining unit determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that a determining unit can be construed to be a number of components of the system of Kitamura. For example, as described above, the system identifies the condition of a particular piece of equipment as well as how many items individually or in lots are being produced at which piece of equipment. The system of Kitamura necessarily must detect information about the manufacturing process through a particular means, otherwise, it would not work. See also col. 5, lines 12-27, as well as figures 11-13. Note element 1304 in figure 13, which "verifies the process procedure".)"

The outstanding Office Action substantiates its position by citing column 5, lines 12-27 of

Kitamura, which portion has specifically stated in its entirety that:

"Referring to FIG. 4, an equipment group code data base 401, 401A prepared by grouping the same processing equipment, is linked with a condition code data base 402, 402A storing the content of the processing and the equipment number(s) of the equipment capable of executing the processing, for each equipment group code, and is also linked with a working history data base 403, 403A storing, for each working, the equipment number(s) of the equipment(s) capable of executing the work. An entry of the condition code data base 402 includes, for each condition code, a field for storing the equipment number of the equipment capable of executing the processing (if execution is possible, large circle is marked) and a field for storing the working content. An entry of the working history data base 403 includes a field for storing the working content and a field for storing the working equipment number."

As illustrated again, in neither the stated Office position nor the Office asserted portion of Kitamura is there any teaching or suggestion of fractional material being utilized in this part of the manufacturing system or process.

As has been consistently shown, numerous parts of the claimed invention are concerned with



U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

and work in conjunction with the fractional printed wiring board. None of the Office stated positions and none of the asserted portions of the asserted prior art teach or suggest any fractional printed wiring board or related system or process. Therefore, the claimed invention is not rendered obvious by the asserted prior art. The Office has also not provided a *prima facie* case of obviousness.

Section 2143 of the MPEP has specifically stated that:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Therefore, it is both a court position and a Patent Office position that to establish a *prima facie* case of obviousness, 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Should the Office find other prior art references but is either unable to identify each and every aspect of the above-mentioned claimed features therein, or the formulated rejection simply would not rise to a level objectively fulfilling all three criteria of establishing a *prima facie* case of

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

obviousness, it is respectfully submitted that the obviousness rejection would be defective and allowance of the claimed invention is requested.

**Claims 7 and 8 are rejected under 35 USC §103(a) as being unpatentable over Kitamura in view of Shin et al.**

As has been shown in the response to the previous rejection, independent claims 1 and 9 are patentably distinguished over the asserted prior art. All claims dependent thereon, by virtue of inherency, are also patentably distinguished over the asserted prior art.

Reconsideration and withdrawal of this rejection are respectfully requested.

U.S. Patent Application Serial No. 09/715,081  
Attorney Docket No.: 001542

**Conclusion**

In view of the aforementioned amendments and accompanying remarks, claims 1 and 9, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Michael N. Lau  
Attorney for Applicant  
Reg. No. 39,479

MNL/alw:lms

Atty. Docket No. 001542  
Suite 1000, 1725 K Street, N.W.  
Washington, D.C. 20006  
(202) 659-2930



23850

PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

Q:\FLOATERS\M\L\001542\2ND OA DRAFT AMENDMENT

**VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/715,081**

**IN THE CLAIMS:**

Please amend claims 1 and 9 as follows:

1. (Twice Amended) A manufacturing system for manufacturing printed wiring boards of plural types, said printed wiring boards scheduled to be manufactured are laid out on at least one predetermined manufacturing block, comprising:

a schedule data storage unit storing manufacturing schedule data including printed wiring board data including each type of the printed wiring boards and the number of each of the printed wiring boards scheduled to be manufactured;

a detecting unit detecting a fractional printed wiring board which should be laid out to a single predetermined manufacturing block together with a printed wiring board having a different type within the printed wiring boards scheduled to be manufactured on the basis of the manufacturing schedule data stored in said schedule data storage unit;

a condition data storage unit storing manufacturing condition data for laying out printed wiring boards of different types on a single predetermined manufacturing block;

a grouping unit grouping each fractional printed wiring board detected by said detecting unit into any of groups according to the manufacturing condition data stored in said condition data storage unit; and

a determining unit determining, per group, layout to at least one predetermined manufacturing block of the fractional printed wiring board.

9. (Twice Amended) A manufacturing method for manufacturing printed wiring boards of plural types, said printed wiring boards scheduled to be manufactured are laid out [to] on at least one predetermined manufacturing block, comprising:

reading manufacturing schedule data including printed wiring board data including each type of the printed wiring boards and the number of each of the printed wiring boards scheduled to be manufactured;

detecting a fractional printed wiring board which should be laid out to a single predetermined manufacturing block together with a printed wiring board having a different type within the printed wiring boards scheduled to be manufactured on the basis of the manufacturing schedule data;

reading a manufacturing condition data for laying out printed wiring boards of different types on a single predetermined manufacturing block;

grouping each detected fractional printed wiring board into any of groups according to the manufacturing condition data; and

determining, per group, layout to at least one predetermined manufacturing block of the fractional printed wiring board.